AMENDMENT TO THE SPECIFICATION

Please amend the title of the application as follows:

VIRTUAL R0 REGISTER FOR AN INSTRUCTION SET ARCHITECTURE WITHOUT AN R0 REGISTER

Please add paragraph 6 on page 4 of the specification under Brief Description of the Drawings to read as follows:

Figure 3 is sample trace cache lines of zero-generating instructions for register r5.

Please replace paragraph 5 on page 5 of the specification under Detailed Description with the following amendment.

Without a zero-generating r0 register, compilers and assembly language programmers must use other means of creating a value of zero. Those of ordinary skill in the art will recognize the following examples, also shown in Figure 3, are but a few of the many techniques for zeroing register r5:

XOR r5, r5, r5

SUB r5, r5, r5

MUL r5, r5, 0x0

MOV r5, 0x00000000